SPECIFICATION AMENDMENTS

Please amend the title to read:

AN IMAGE SENSING APPARATUS ARRANGED ON A SINGLE SUBSTRATE

Please amend the paragraph at page 14, lines 1-18, as follows:

Fig. 3 is a schematic view showing a structure of one pixel 1d in the pixel unit. Fig. 8 is a schematic view showing another structure of a pixel in the pixel unit. Referring to Fig. 3, the pixel has a buried photodiode PD, transfer MOS transistor TX for transferring signal charges from the buried photodiode PD, floating diffusion region FD (charge/voltage conversion unit) where the transferred signal charges are held, amplification MOS transistor SF with a gate connected to the floating diffusion region FD, selection MOS transistor ~~SE~~ SEL, and reset MOS transistor RES for resetting the floating diffusion region FD and amplification MOS transistor SF. The selection MOS transistor SEL builds a source follower circuit together with an MOS transistor M having a constant current source. Referring to Fig. 8, the selection MOS transistor SEL and amplification MOS transistor SF are replaced with each other.

Please amend the paragraph at page 25, lines 4-19, as follows:

The power supply voltage of a sensor block 1 is set at 6.5 V, and that of a signal processing block 2 is set at 3.3 V. In this embodiment, the sensor block 1 and signal processing block 2 have a power supply voltage difference. Hence, as shown in Fig. 12, a level shift circuit ~~1d~~ 1e for level-shifting the signal from a horizontal scanning unit 1c is prepared, and the output from the level shift circuit ~~1d~~ 1e is connected to an amplifier unit 2a. The level shift circuit need not be always used in the sensor block 1. This circuit may

be inserted between the sensor block 1 and signal processing block 2 or in the signal processing block 2. The degree of freedom in design is higher when the level shift circuit is in the sensor block where the power supply voltage is high, and the input and output ranges are wide.

Please amend the paragraph at page 31, line 6 through page 32, line 2, as follows:

Fig. 19 is a block diagram showing the arrangement of an image sensing apparatus according to the 10th embodiment of the present invention. In this image sensing apparatus, a sensor system 10 constructed by an image sensor 12 and driving circuit 13 therefor has one independent power source 11. A data processing system 14 having an A/D conversion unit 16 for A/D-converting an image sensing data signal from the image sensor 12 and DSP unit 17 for performing arithmetic operation while storing the data in a memory 18 has an independent power source 15. An output processing system 19 also has a power source 20, in which a plurality of memories 22 and 23 are prepared to convert the image sensing data from the data processing system 14 into a data structure compatible with the output apparatus 31, and an encoder 21 encodes the data to display, communicate, or record it. An AE/AF system 24 where AE/AF conditions for image sensing are calculated by an AE/AF processing unit 26 also has a power source 25. The operation mode is identified in accordance with the signal from an operation unit 30 of the apparatus, and a system control unit 28 including a memory 29 determines the ON/OFF timing of power supply to each processing system.

Please amend the paragraph at page 38, lines 10-27, as follows:

Fig. 23 is a block diagram showing the arrangement of a solid-state image sensing apparatus according to the 11th embodiment of the present invention. In this image sensing apparatus, a sensor system 210 constructed by an image sensor 212 and driving circuit 213 therefor has one independent clock control unit 211. A data processing system 214 has an A/D conversion unit 216 for A/D-converting an image sensing data signal from the image sensor 212 and DSP unit 217 for performing arithmetic operation while storing the data in a memory 218. The data processing system 214 also has a clock control unit 215. An output processing system 219 has a clock control unit 220, a plurality of memories 222 for converting the image sensing data from the data processing system 214 into a data structure compatible with the output apparatus 231, and an encoder 221 for encoding the data to display, communicate, or record it.

Please amend the paragraph at page 41, lines 1-7, as follows:

Referring to Fig. 25, a clock generator 239 is prepared in the system control unit 228 or a block not shown in Fig. 22. Different kinds of clock signals from a 100% clock generator 233, 50% clock generator 232, and 25% clock generator ~~231~~ 240 are selected by a selection switch 234 and output to input clock terminals 235 to 238 of the processing systems.